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ELECTROTHERMAL SIMULATION OF POWER VDMOS TRANSISTORS

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ABSTRACT

Poisson's equation and the electron continuity equation, together with heat flow equation are solved self-consistently to obtain the lattice temperature profile under non-isothermal conditions in a power VDMOS transistor. The effect of the variable lattice temperature on the forward characteristics of VDMOSTs is presented, and discussed. The results show that self-heating in power VDMOSTs has a significant effect. The thermal coupling effects on the forward I–V characteristics are compared and discussed between the power VDMOST and the conventional MOSFET.

KEY WORDS Power VDMOS transistor Lattice temperature Non-isothermal and isothermal Numerical simulation MOSFET

INTRODUCTION

The characteristics of power VDMOS transistors (VDMOST) make them important candidates for many applications in electronic circuits and systems. They are being used in audio/radiofrequency circuits and high-frequency inverters such as those used in switched mode power supplies. Several industrial application areas (e.g. automobile and aircraft engine industries) require the reliable operation of the power VDMOST in a high temperature environment. This makes it necessary to understand the behaviour not only at ambient isothermal temperature but also under non-isothermal internal conditions. Several papers have studied the high temperature performance of VDMOSTs under isothermal conditions, including the effect on the on-resistance, transconductance, threshold voltage, and forward I–V characteristics[1,2]. However, few studies have reported on non-isothermal lattice temperature distribution due to self-heating in the bulk of the device, and its effect on the characteristics of the VDMOST[3]. In this paper, Poisson's equation and the electron continuity equation are solved self-consistently with the heat-flow equation, with appropriate physical models representing temperature dependent saturation velocity of electrons and temperature-dependent bandgap forward I–V characteristics are presented for the VDMOST under both conditions and compared with those for the conventional low-voltage MOSFET. Differences in the effect of self-heating between the two cases are presented and discussed.

TWO-DIMENSIONAL SELF-CONSISTENT NUMERICAL MODEL

Basic equations[5]

The electrothermal behaviour of power semiconductor devices is governed by the device equations consisting of Poisson's equation:

$$\nabla \cdot (\varepsilon_s \nabla \psi) = -q(p - n + N_D^+ - N_A^+) \tag{1}$$

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the electron continuity equation:

$$-\frac{1}{q}\nabla\cdot J_n = G - R \tag{2}$$

the hole continuity equation:

$$\frac{1}{q}\nabla\cdot J_p = G - R \tag{3}$$

and the heat flow equation:

$$\nabla\cdot(\kappa\nabla T) = -P \tag{4}$$

where ψ is the electrostatic potential, N_D^+, N_A^- the ionised donor and acceptor impurity densities respectively, $(G–R)$ are net generation, and P and κ the heat generation and thermal conductivity, respectively.

The current densities in (2) and (3) are given by:

$$J_n = -q\mu_n n\nabla\phi_n \tag{5}$$

$$J_p = -q\mu_p p\nabla\phi_p \tag{6}$$

where the thermally driven currents have not been included. μ_n and μ_p are the mobilities of electrons and holes, ϕ_n and ϕ_p are the quasi-Fermi potentials for electrons and holes.

Physical models

Two recombination mechanisms, namely Shockley–Read–Hall (SRH) and Auger recombination, are included in the simulation. SRH recombination is expressed by:

$$R - G = \frac{np - n_{ie}^2}{\tau_p(n + n_{ie}) + \tau_n(p + n_{ie})} \tag{7}$$

and Auger recombination by:

$$R - G = (2.8 \times 10^{-31}n + 9.9 \times 10^{-32}p)(pn - n_{ie}^2) \tag{8}$$

where τ_n and τ_p are the recombination lifetimes for electrons and holes, τ_n and τ_p are taken to be equal at 0.5 μs, n_{ie} is the effective intrinsic carrier concentration. The temperature dependence of the bandgap model has been included in the above recombination models[6]:

$$E_g(T) = 1.170 - \frac{4.73 \times 10^{-4}T^2}{T + 636}\text{eV} \tag{9}$$

A field dependent mobility model, in which the lattice temperature dependence and doping dependence of low field mobility are taken into account, is defined as:

$$\mu = \frac{\mu_{LF}}{\left[1 + \left(\frac{\mu_{LF}\nabla\phi_{n,p}}{v_{\text{sat}}(T)}\right)^{\beta}\right]^{1/\beta}} \tag{10}$$

where E is magnitude of electrical field, and the low field mobility μ_{LF} is expressed as:

$$\mu_{LF} = \mu_{\min} + \frac{\mu_0\left(\frac{T}{300}\right)^{-\alpha_1} - \mu_{\min}}{1 + \left(\frac{N}{N_{\text{ref}}}\right)^{\alpha_2}} \tag{11}$$

where N is the net doping concentration, μ_0 is a constant mobility factor for electrons or holes, T is lattice temperature, μ_{min}, N_{ref}, α_1, α_2, β are constants. In our simulation, $\mu_{min} = 92.0\ cm^2/V\text{-}s$, $N_{ref} = 1.30E17/cm^3$, $\alpha_1 = 2.42$, $\alpha_2 = 0.91$ and $\beta = 2.0$ are chosen for electrons.

Finally, a temperature dependent saturation velocity for electrons[1,7] is introduced into (10), given by:

$$v_{sat}(T) = 1.434 \times 10^9 T^{-0.87}\ cm/s \tag{12}$$

Heat generation within the semiconductor in our simulation is given by[5,8]:

$$P = J \cdot E + (R - G)(E_g + \tfrac{3}{2}kT) \tag{13}$$

The first term represents Joule heating, and the second recombination heating. Equation (13) does not include the effect of temperature variations on the heat dissipation nor the effect of bandgap narrowing.

Numerical method

Equations (1) to (4) are discretized by means of the box integration discretization scheme known as the control region approximation (CRA) introduced by Board and Mawby[5], based on a triangular mesh. The resulting non-linear discretized equation set is solved using the Newton–Raphson method, and the underlying linear equations are solved by the conjugate gradient squared algorithm (CGS). Because the VDMOST is a unipolar device, only Poisson's and the electron continuity equations together with heat flow equation are solved for the n-channel VDMOST in our study using the same solution scheme[5].

RESULTS AND DISCUSSION

Lattice temperature profiles due to self-heating

The cross-section of the VDMOST analysed here is shown in *Figure 1a*. The triangular mesh, on which the discretization is taken, is given in *Figure 1b*. The log of doping concentration throughout the device is illustrated in *Figure 2*. By making use of the self-consistent numerical procedure discussed above, the lattice temperature distributions in VDMOST with idealized thermal boundary conditions at the drain are shown in *Figure 3*, where the heat sink temperatures are 300 and 400 K, and the biases of gate and drain contact are 20.0 and 4.5 V. The peak temperature is located near the channel region. This is because the electric field component, which is parallel to the direction of the current density vector, and the current density are highest near the end of the n-channel for the VDMOST. This results in the Joule heating reaching its maximum at that point. From the above results, we can conclude that the self-heating in power VDMOST cannot be ignored. The peak values of lattice temperature will increase as the biases of the drain contact increase. Shown in *Figure 4* are the peak lattice temperatures in the VDMOST as a function of drain bias, with different heat sink temperatures. It can be seen that the increase of lattice temperature becomes small for high drain biases, which results from the current saturation in the VDMOST.

Forward I–V characteristics under non-isothermal conditions

The forward I–V characteristics of the device under isothermal and non-isothermal conditions with different heat sink temperatures are presented in *Figure 5*. It can be seen that the forward characteristics of VDMOSTs are changed when variable lattice temperatures are taken into account. It is interesting to note that the current of VDMOSTs under non-isothermal conditions is at first higher than the current under isothermal conditions, but as the drain bias increases it

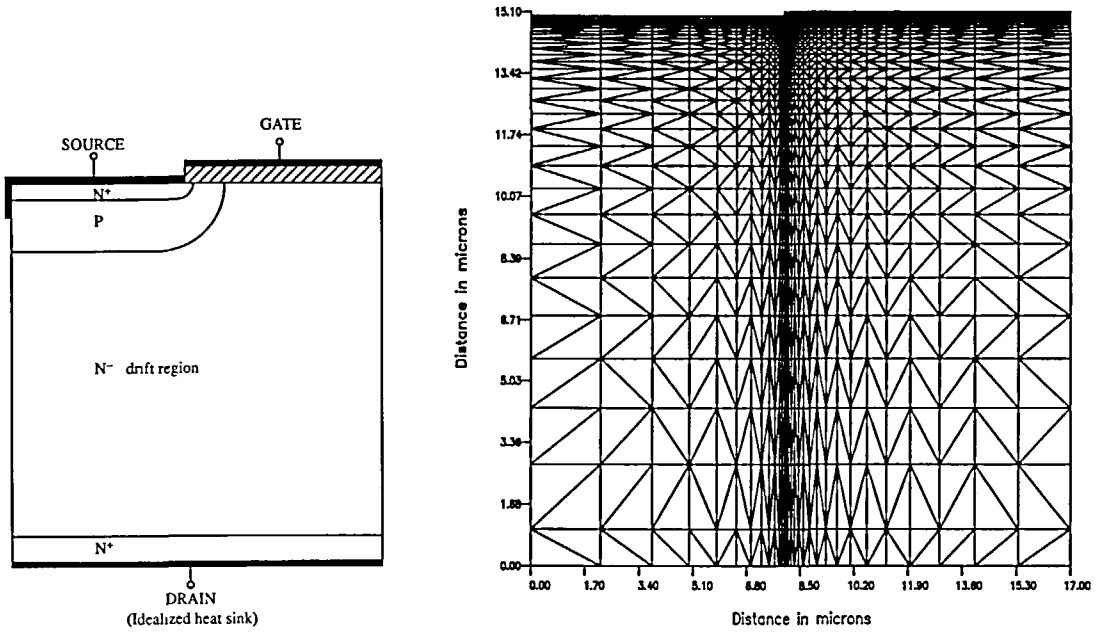

Figure 1 (a) Power VDMOST cross-section. (b) Finite element mesh of VDMOST

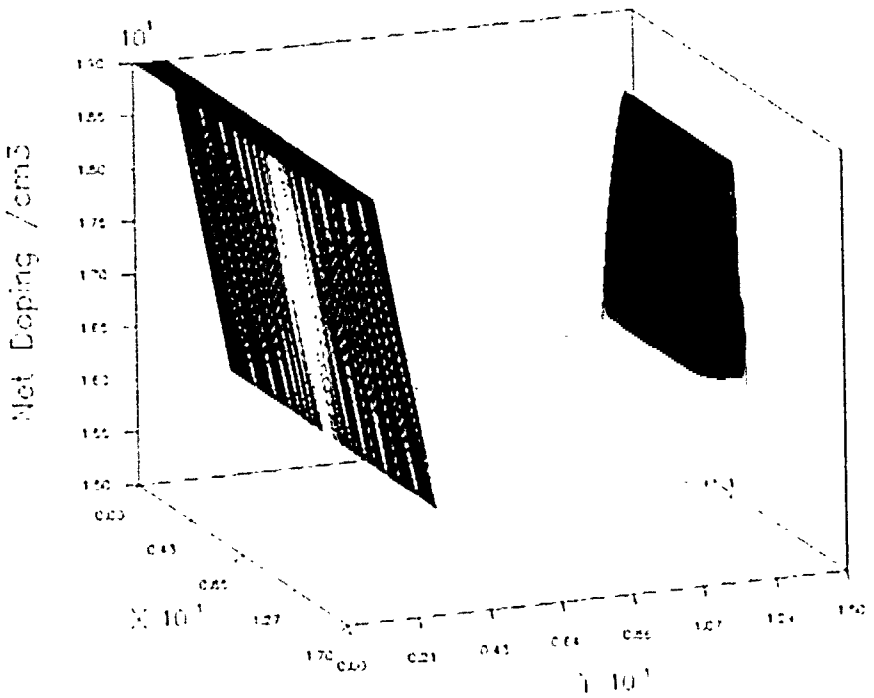

Figure 2 Doping profile of VDMOST

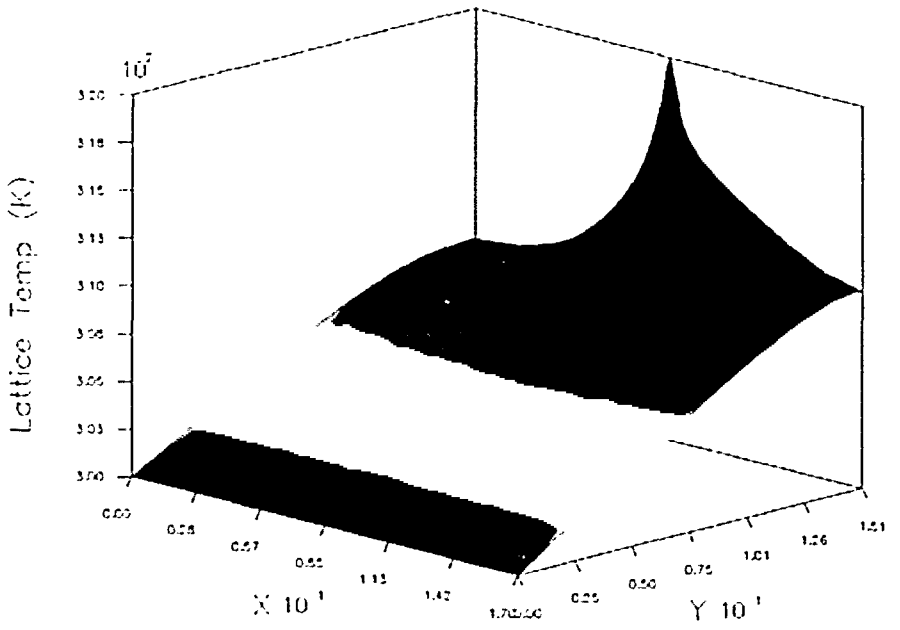

Figure 3a Lattice temperature distribution due to self-heating of VDMOST for idealized heat sink at the drain. The voltage of the gate and drain are 20.0 V and 4.5 V, respectively

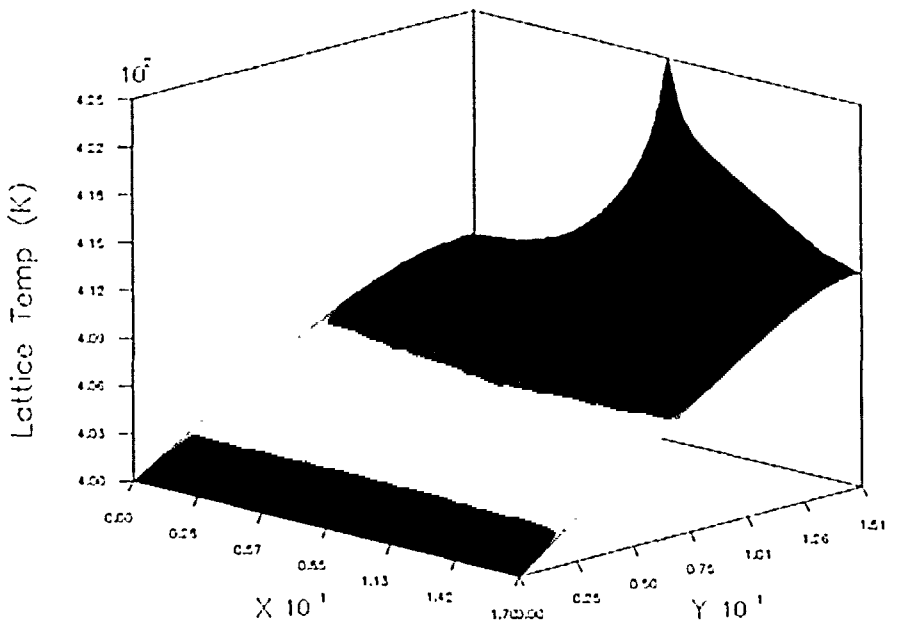

Figure 3b Lattice temperature distribution due to self-heating of VDMOST for idealized heat sink at the drain, where the temperature of heat sink is 400 K. The voltage of the gate and drain are 20.0 V and 4.5 V, respectively

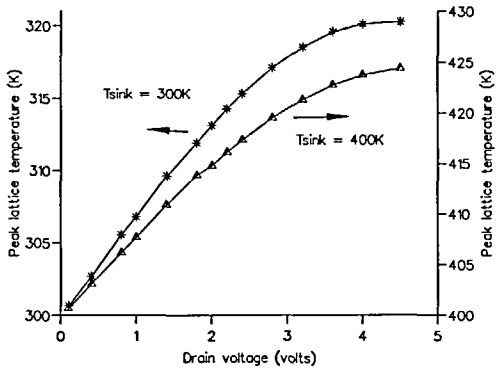

Figure 4 Peak lattice temperature as a function of the drain voltages

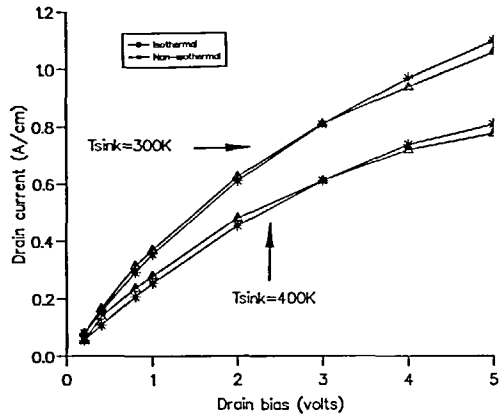

Figure 5 Forward I–V characteristics of VDMOSTs under isothermal and non-isothermal condition. The voltage of the gate is 20.0 V

crosses over and becomes lower. These results are confirmed by the experimental curve in Reference 3. This situation is different from that found in the conventional MOSFETs, where the current under non-isothermal conditions is always lower than that when no thermal coupling is taken into account. *Figure 7* shows the results for the conventional MOSFET shown in *Figure 6*. The lattice temperature profile is given in *Figure 7a*, where the idealized heat sink is located at the substrate. The effect of variable lattice temperature on the forward I–V characteristics for the MOSFET is presented in *Figure 7b*. It can be seen that the peak lattice temperature is also located near the end of the channel region, but the current under non-isothermal conditions is always less than the current under isothermal conditions. This difference in behaviour between power VDMOST and conventional MOSFET can be understood by the following argument. For a conventional MOSFET, the on-resistance in the linear operating region is given by:

$$R_{ch} = A\mu_n(V_G - V_T) \tag{14}$$

where μ_n is the electron mobility, A is a constant determined by the width and length of channel and the gate oxide capacitance, V_G is the bias of the gate contact and V_T is threshold voltage of the MOSFET. Both the threshold voltage V_T and the electron mobility μ_n decrease with increase of lattice temperature. This means that μ_n decreases, but $(V_G - V_T)$ increases in (14). From the results of Reference 9, a linear variation of V_T with temperature is expected, and the change of V_T with temperature is very small compared with the change of electron mobility μ_n. For example, for a n-channel MOSFET, the threshold voltage V_T only decreases by about 0.1 V when the temperature increases from 273 to 423 K, whereas the mobility changes by about 1116 cm^2/V-s. Thus the on-resistance of a normal MOSFET is mainly determined by the carrier mobility. The later will decrease rapidly with the increase of lattice temperature and electric field. As the drain bias increases, the lattice temperature and electric field will increase, resulting in the channel resistance R_{ch} increasing further. This in turn leads to the forward current under non-isothermal conditions always being lower than the current under isothermal condition. The situation for the power VDMOST is different. Its on-resistance is dominated by the resistance of the drift region R_D[10], which has the following relation with electron mobility μ_n and electron concentration:

$$R_D \propto \mu_n \times n \tag{15}$$

where n is electron concentration in the N-drift region. As the drain bias is increased, the lattice temperature will increase, leading to a decrease in μ_n, whereas n increases with temperature. At

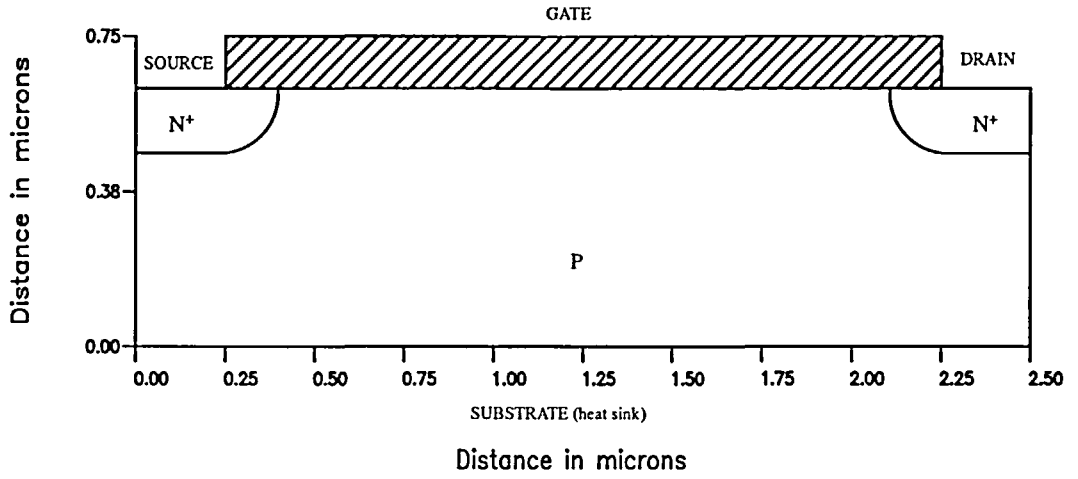

Figure 6 MOSFET cross-section

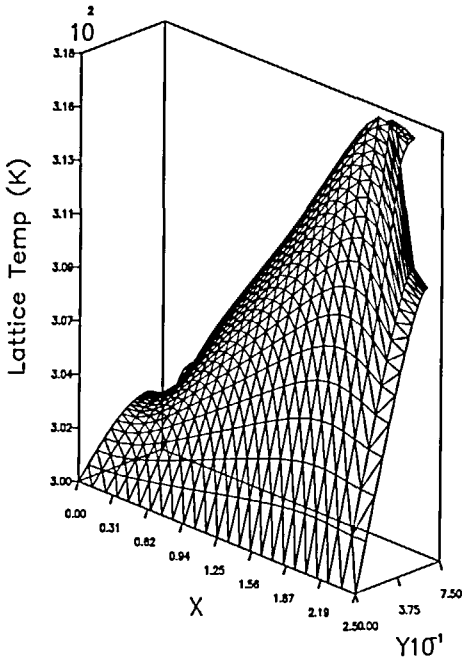

Figure 7a Lattice temperature distribution due to self-heating of MOSFET for idealized heat sink at the substrate. The voltage of the gate and the drain are 10.0 V and 4.0 V, respectively

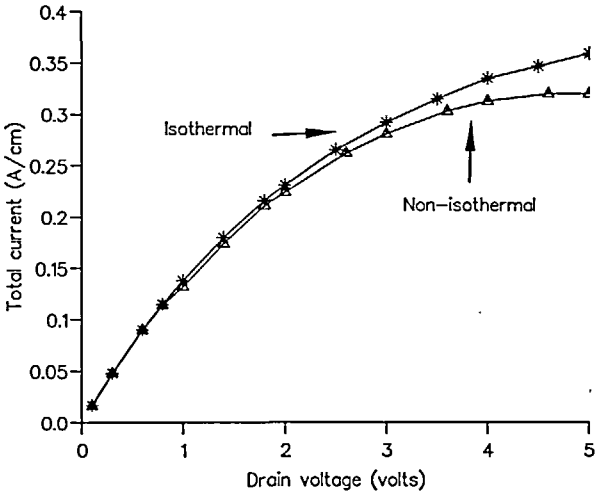

Figure 7b Forward I–V characteristics of MOSFETs under isothermal and non-isothermal condition. The voltage of the gate is 10.0 V

low biases on the drain, the decrease in μ_n cannot match the increase in n, which results in the forward current under non-isothermal conditions being higher than that current under isothermal conditions at low drain bias. As the bias of the drain contact continues to increase, the electric field and lattice temperature in the drift region both increase, leading to further reduction in μ_n,

and the disparity between the changes in n and μ_n will become less. At a particular drain bias, the decrease in μ_n will exceed the increase in electron concentration n. Also, as the lattice temperature increases, the resistance of the n-channel region will become significant. These effects taken together mean that forward current is lower under non-isothermal conditions than under isothermal conditions at high drain biases, as shown in *Figure 5*.

CONCLUSIONS

Self-heating in the power VDMOST has been shown to have a significant effect on the forward characteristics, with strong Joule heating occurring near the channel region. The effect of the variable lattice temperature due to self-heating in the bulk regions between power VDMOSTs and conventional MOSFETs is different. For conventional MOSFETs, the forward current under non-isothermal conditions is always lower than the current under isothermal conditions, whereas for the power VDMOS transistor, the forward current at low drain bias is higher under non-isothermal conditions than that with no thermal coupling, and at high drain bias will become lower than the current in the isothermal case.

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